input data and the output data in converting the sampling frequency, includes a storage device 13 for continuously writing the input data or the data obtained by over-sampling the input data and for continuously reading out the data written maintaining a predetermined address difference relative to the writable address, and an interpolation processing unit 14 for interpolating the data read-out from the storage device 13 to obtain data of which the sampling frequency is converted. In converting the sampling frequency, an address difference between a writable address and a readable address in the storage device 13 is optimized, the address difference being optimized without limitation for a predetermined period of time from the start of supplying the input data and, then, being optimized by imposing a predetermined limitation after the passage of the predetermined period of time.--

A1 Cont.

IN THE CLAIMS

Please amend claims 1-11 by rewriting same to read as follows:

--1. (Amended) A sampling frequency conversion apparatus for converting input data of a first sampling frequency into output data of a second sampling frequency, comprising:

storage means into which said input data are

A2 Cont.

continuously written and read-out;

interpolation processing means for interpolating the data read-out from said storage means to obtain the data of said second sampling frequency;

address difference detecting means for detecting an address difference between a writable address and a readable address in said storage means; and

address control means for performing an optimization operation optimizing the address difference detected by said address difference detecting means, wherein

said address control means adaptively sets a limitation on the optimizing operation.

A2 cont

--2. (Amended) The sampling frequency conversion apparatus according to claim 1, wherein

said address control means works so as not to execute the optimization operation when the address difference detected by said address difference detecting means falls within a predetermined range after passage of a predetermined period of time from a starting time when the input data is supplied.

--3. (Amended) The sampling frequency conversion apparatus according to claim 1, wherein

said address control means works so as not to execute the optimization operation when the address difference detected by said address difference detecting means falls

within a predetermined range after passage of a predetermined period of time from a time when the power source circuit is switched on.

--4. (Amended) The sampling frequency conversion apparatus according to claim 1, wherein

said predetermined period of time is longer than a time required for stabilizing a ratio between the first sampling frequency of the input data and the second sampling frequency of the output data after a start of supplying said input data.

Az Cont.

~~--5.~~ (Amended) The sampling frequency conversion apparatus according to claim 1, wherein

said address control means works so as not to execute said optimization operation when the address difference detected by said address difference detecting means falls within a predetermined range after passage of a predetermined period of time from a time when the input data is initially supplied.

--6. (Amended) The sampling frequency conversion apparatus according to claim 1, wherein

said address control means performs a control operation to bring said address difference close to a predetermined optimum value imposing no limitation when a predetermined period of time has not been passed after a start

of supplying said input data or when the address difference detected by said address difference detector means falls outside of a predetermined range.

--7. (Amended) The sampling frequency conversion apparatus according to claim 6, wherein

said address control means executes the control operation by bringing the address difference close to the predetermined optimum value by judging that a moment at which the changing address difference value exceeds the predetermined optimum value or becomes smaller than the predetermined optimum value, is the moment of an optimum address difference.

A2 Cont.

--8. (Amended) A sampling frequency conversion apparatus having a plurality of sampling frequency conversion means for converting a first sampling frequency of input data into a_second sampling frequency to obtain output data, wherein

each of said plurality of sampling frequency conversion means includes:

storage means into which said input data are continuously written and read-out;

interpolation processing means for interpolating the data read out from said storage means to obtain the data of said second sampling frequency;

address difference detecting means for detecting an

address difference between a writable address and a readable address in said storage means;

and address control means for performing an optimizing a action operation optimizing the address difference detected by said address difference detection means, wherein

said address control means works so as not to execute the optimization operation when the address difference detected by the address difference detector means in each of said plurality of sampling frequency conversion means falls within a predetermined range after passage of a predetermined period of time from a start of supplying said input data, thereby to eliminate a time difference between the output data from said plurality of sampling frequency conversion means.

A2 Cont.

--9. (Amended) The sampling frequency conversion apparatus according to claim 8, wherein

said predetermined period of time is longer than a time required for stabilizing a ratio between the first sampling frequency of the input data and the second sampling frequency of the output data after a start of supplying the input data.

--10. (Amended) The sampling frequency conversion apparatus according to claim 8, wherein

said address control means performs a control operation to bring said address difference close to a predetermined optimum value when a predetermined period of

time has not passed after the start of supplying said input data or when the address difference detected by said address difference detecting means falls outside of the predetermined range.

A2 cont.

--11. (Amended) The sampling frequency conversion apparatus according to claim 10, wherein

said address control means executes the control operation by bringing the address difference close to the predetermined optimum value by judging that a moment at which the changing address difference value exceeds the predetermined optimum value or becomes smaller than the predetermined optimum value, is the moment of an optimum address difference.

REMARKS

Claims 1-11 remain in the application and have been amended hereby.

As will be noted from the Declaration, Applicants are citizens and residents of Japan and this application originated there.

Accordingly, the amendments to the specification are made to place the application in idiomatic English, and the claims are amended to place them in better condition for examination.

An early and favorable examination on the merits is